

AMENDMENT UNDER 37 C.F.R. § 1.111
APPLICATION NO. 10/058,804
ATTORNEY DOCKET NO. Q68166

IN THE CLAIMS:

1. (Currently Amended) Phase locked loop charge pump comprising:
a drain node; ~~(A, B)~~ and
at least a cascode transistor ~~(M4, M6)~~ for limiting the variation of the voltage of said drain node, ~~CHARACTERISED IN THAT~~
wherein an intermediate switch transistor ~~(M3, M5)~~ is placed between the drain node ~~(A, B)~~ and the cascode transistor ~~(M4, M6)~~.
2. (Currently Amended) The charge pump of claim 1, said charge pump comprising a first node ~~(A)~~, a second node ~~(B)~~, a branch connecting the first node with the second node, said branch comprising a first cascode transistor ~~(M4)~~ and a second cascode transistor ~~(M6)~~, a first switch transistor ~~(M3')~~ placed in parallel to the first cascode transistor ~~(M4)~~, and a second switch transistor ~~(M5')~~ placed in parallel to the second cascode transistor ~~(M6)~~, ~~CHARACTERISED IN THAT~~ further comprising at least an intermediate switch transistor ~~(M3, M5)~~ is placed between the drain node ~~(A, B)~~ and a cascode transistor ~~(M4, M6)~~; in parallel to one of the first switch transistor ~~(M3')~~ or to and the second switch transistor ~~(M5')~~.
3. (Currently Amended) The charge pump of claim 2, ~~CHARACTERISED IN THAT it comprises further comprising~~ two intermediate switch transistors ~~(M3, M5)~~, a first intermediate transistor ~~(M3)~~ being placed between the first node ~~(A)~~ and the first cascode transistor ~~(M4)~~, said first intermediate transistor ~~(M3)~~ being placed in parallel to the first switch transistor ~~(M3')~~, while the second intermediate switch transistor ~~(M5)~~ being placed between the second node ~~(B)~~ and the second cascode transistor ~~(M6)~~, said second intermediate transistor ~~(M5)~~ being placed in parallel to the second switch transistor ~~(M5')~~.

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4. (Currently Amended) The charge pump of claim 3, ~~CHARACTERISED IN THAT~~
wherein the first switch transistor (~~M3'~~) in parallel to the first cascode transistor (~~M4~~) and/or the
second switch transistor (~~M5'~~) in parallel to the second cascode transistor (~~M6~~) is connected to a
further cascode transistor (~~M4', M6'~~) in parallel to the first and/or second cascode transistor
(~~M4, M6~~).

5. (Currently Amended) The charge pump of claim 4, ~~CHARACTERISED IN THAT~~
wherein the first switch transistor (~~M3'~~) in parallel to the first cascode transistor (~~M4~~) and a
further cascode transistor (~~M4'~~) form a dummy branch in parallel to the first cascode transistor
(~~M4~~) and the first intermediate transistor (~~M3~~), said dummy branch having connections so as to
be controlled by the complement signal of the signal controlling the first intermediate transistor
(~~M3~~) and/or the second switch transistor (~~M5'~~) in parallel to the second cascode transistor (~~M6~~)
and a further cascode transistor (~~M6'~~) form a dummy branch in parallel to the second cascode
transistor (~~M6~~) and the second intermediate transistor (~~M5~~), said dummy branch having
connections so as to be controlled by the complement signal of the signal controlling the second
intermediate switch transistor (~~M5~~).

6. (Currently Amended) ~~Electronic~~ An electronic ~~and/or integrated~~ circuit comprising a
charge pump according to claim 1.

7. (New) An integrated circuit comprising a charge pump according to claim 1.

8. (New) A phase locked loop charge pump comprising:
a drain node;
a first cascode transistor to limit the variation of the voltage of said drain node;
a first intermediate switch transistor positioned between said drain node and said first cascode
transistor; and

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cont a dummy branch with a second cascode transistor connected to a second intermediate switch transistor,

wherein said second intermediate switch transistor is positioned between said first node and said second cascode transistor.
